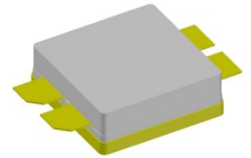


Product Features

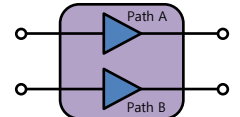
- 1880~2025MHz
- 195W Saturated Power @ 48V
- 48% Drain Efficiency @ 45dBm
- Internally Matched
- Asymmetrical Doherty GaN HEMT

Applications

- WiMAX, LTE, WCDMA, GSM
- Multi-Band, Multi-Mode
- Multi-Carrier
- High Efficiency, Doherty Amplifier



Package Type : RF12001DKR3

Typical Single-Carrier LTE Performance ($V_{DS} = +48V$, $T_C = 25^\circ C$, 50Ω)

Frequency [MHz]	Peak Power	Average Power ^{*1}			
	Power [W]	Power [W]	Gain [dB]	Drain Efficiency [%]	ACLR [dBc]
1885.0	207.5	32	15.9	47.8	-28.3
1952.5	200.9	32	16.9	49.9	-27.8
2020.0	187.9	32	16.3	49.3	-27.8

Note

*1 Measured in the IE19195WD Doherty test board amplifier circuit, under LTE 10MHz, PAR 7.5dB @0.01% probability on CCDF

Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Condition
Drain to Source Voltage	V_{DSS}	150	V	$T_C = 25^\circ C$
Gate to Source Voltage	V_{GS}	-10, +2	V	$T_C = 25^\circ C$
Operating Voltage	V_{DD}	52	V_{DC}	-
Storage Temperature	T_{STG}	-65, +150	$^\circ C$	-
Case Operating Temperature	T_C	-40, +150	$^\circ C$	30 seconds
Operating Junction Temperature ^{*1}	T_J	225	$^\circ C$	-
Soldering Temperature ^{*2}	T_S	245	$^\circ C$	-

Note

*1 Continuous use at maximum temperature will affect MTTF.

*2 Refer to the Application Note(AN-002) on soldering - "Solder Condition for RFHIC's GaN Device"

Thermal Characteristics

Rating	Symbol	Value	Unit	Condition
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.90 ^{*1}	$^\circ C/W$	$T_C = 85^\circ C$

Note

*1 Measured for the IE19195WD at dissipation power is 48.3W

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
DC Characteristics - Path A (Carrier) ^{*1}						
Maximum Forward Gate Current	T _c = 25℃	I _{GMAX}	-	-	12.0	mA
Maximum Drain Current ^{*2}	T _c = 25℃	I _{DMAX}	-	-	4.5	A
Power Dissipation	T _c = 85℃	P _{DMAX}	-	-	48.3	W
Gate Threshold Voltage	V _{DS} = 10V	V _{GS(TH)}	-3.8	-3.0	-2.3	V _{DC}
	I _D = 10.8mA					
Gate Quiescent Voltage	V _{DS} = 48V	V _{GS(Q)}	-	-2.8	-	V _{DC}
	I _D = 350mA					
Drain-Source Breakdown Voltage	V _{GS} = -8V	V _{BR}	150	-	-	V
	I _D = 10.8mA					
Saturated Drain Current ^{*3}	V _{DS} = 6V	I _{DS}	9.0	10.8	-	A
	V _{GS} = 2V					
Gate Leakage Current	V _{GS} = -8V	I _{GLKG}	-2.4	-	-	mA
	V _{DS} = 120V					
Drain Leakage Current	V _{GS} = -8V	I _{DLKG}	-	-	4.3	mA
	V _{DS} = 120V					
DC Characteristics - Path B (Peaking) ^{*1}						
Maximum Forward Gate Current	T _c = 25℃	I _{GMAX}	-	-	16.0	mA
Maximum Drain Current ^{*2}	T _c = 25℃	I _{DMAX}	-	-	6.0	A
Power Dissipation	T _c = 85℃	P _{DMAX}	-	-	57.4	W
Gate Threshold Voltage	V _{DS} = 10V	V _{GS(TH)}	-3.8	-3.0	-2.3	V _{DC}
	I _D = 14.4mA					
Gate Quiescent Voltage	V _{DS} = 48V	V _{GS(Q)}	-	-2.8	-	V _{DC}
	I _D = 45mA					
Drain-Source Breakdown Voltage	V _{GS} = -8V	V _{BR}	150	-	-	V
	I _D = 14.4mA					
Saturated Drain Current ^{*3}	V _{DS} = 6V	I _{DS}	12.0	14.4	-	A
	V _{GS} = 2V					
Gate Leakage Current	V _{GS} = -8V	I _{GLKG}	-3.2	-	-	mA
	V _{DS} = 120V					
Drain Leakage Current	V _{GS} = -8V	I _{DLKG}	-	-	5.8	mA
	V _{DS} = 120V					

Note

*1 Measured on wafer prior to packaging.

*2 Current Limit for long term, reliable operation

*3 Scaled from PCM data.

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
RF Characteristics (Fc=1952.5MHz unless otherwise noted)						
Saturated Output Power ^{*1,4}	V_{DS} = 48V	P _{SAT}	-	195	-	W
	I_{DQ} = 350mA					
Modulated Gain ^{*2}	V_{DS} = 48V	G _{BR}	15.0	16.0	-	dB
	I_{DQ} = 350mA					
	P_{OUT} = 45dBm					
LTE Linearity ^{*2}	V_{DS} = 48V	ACLR	-	-27.0	-24.0	dBc
	I_{DQ} = 350mA					
	P_{OUT} = 45dBm					
Modulated Drain Efficiency ^{*2}	V_{DS} = 48V	η	45.0	48.0	-	%
	I_{DQ} = 350mA					
	P_{OUT} = 45dBm					
Output Mismatch Stress ^{*1, 3}	V_{DS} = 48V	VSWR	-	-	10:1	ψ
	I_{DQ} = 350mA					
	P_{OUT} = P_{SAT} Pulsed					

Note

*1 Pulse width 100μsec, Duty Cycle 10%.

*2 Measured in the IE19195WD Doherty test board amplifier circuit, under LTE 10MHz, PAR7.5dB @0.01% probability on CCDF.

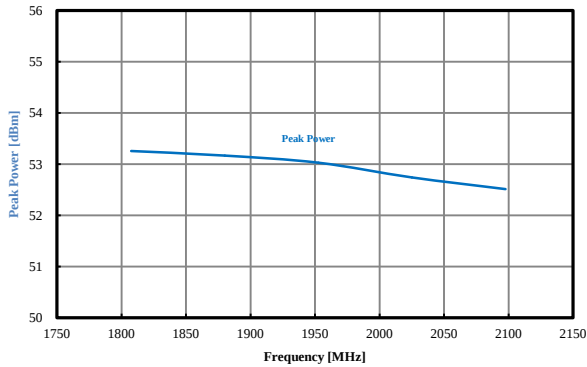
*3 Measured in the IE19195WD Doherty test board amplifier circuit. No damage at all phase angles.

*4 Psat is defined as $\Delta P_{out}/\Delta P_{in} < 0.1$, where ΔP_{in} is increased input power, ΔP_{out} is increased output power.

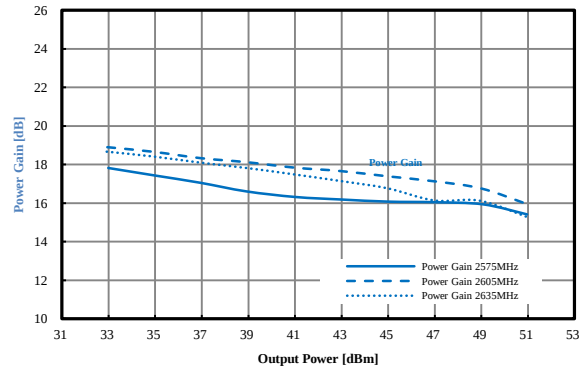
Typical Pulsed Signal Performance

(Tc=25°C, Measured in the IE19195WD test board amplifier circuit)

Peak Power vs. Frequency



Pulsed Power Gain vs. Output Power



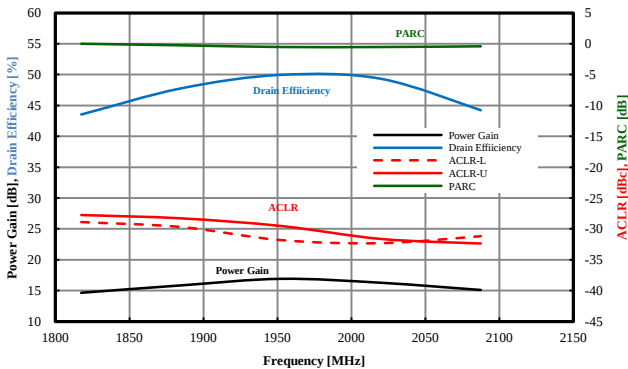
$$V_{DS} = 48V, \quad I_{DQ(C)} = 350mA,$$

$$V_{GS(P)} = -5V, \quad \text{Pulse Width} = 100\mu\text{sec}, \quad \text{Duty Cycle} = 10\%$$

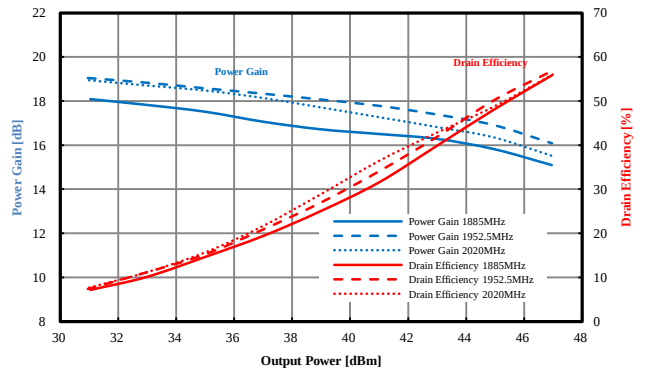
Typical LTE Signal Performance

(Tc=25°C, Measured in the IE19195WD test board amplifier circuit)

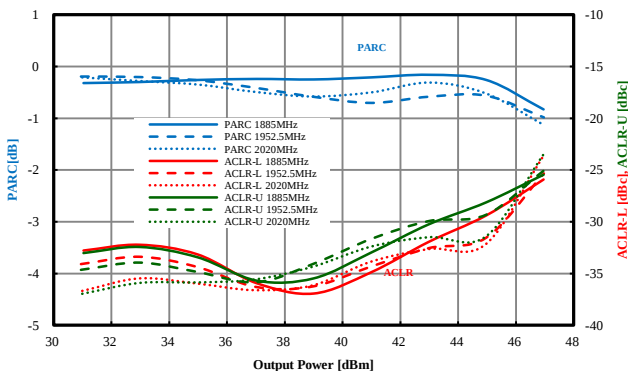
LTE Power Gain, Drain Efficiency, ACLR, PARC vs. Frequency



Power Gain, Drain Efficiency vs. Output Power



PARC, ACLR vs. Output Power



$$P_{AVG} = 45\text{dBm},$$

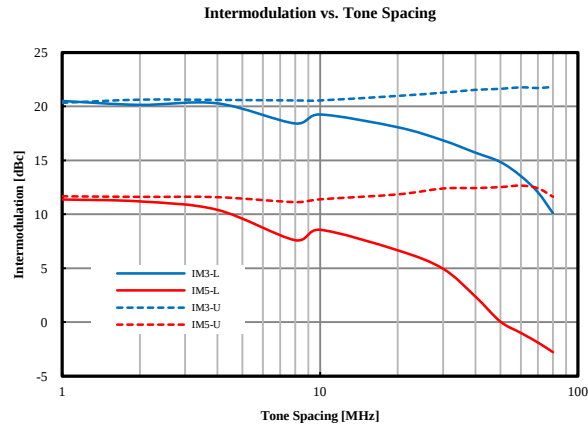
$$V_{DS} = 48V, \quad I_{DQ(C)} = 350mA,$$

$$V_{GS(P)} = -5V$$

LTE 10MHz BW, PAPR=7.5dB @ 0.01% Probability on CCDF

Typical 2-tone Intermodulation Imbalance Performance

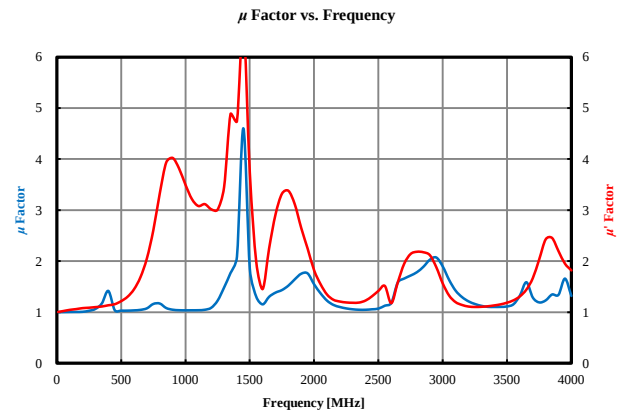
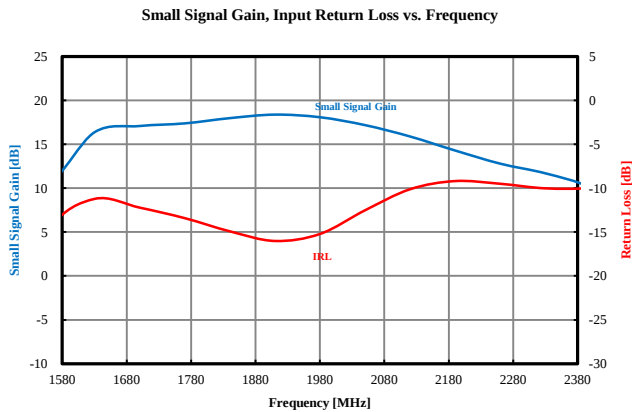
(Tc=25 °C, Measured in the IE19195WD Doherty test board amplifier circuit)



2-tone Power = 50.9dBm, $V_{DS} = 48V$, $I_{DQ(C)} = 350mA$, $V_{GS(P)} = -5V$

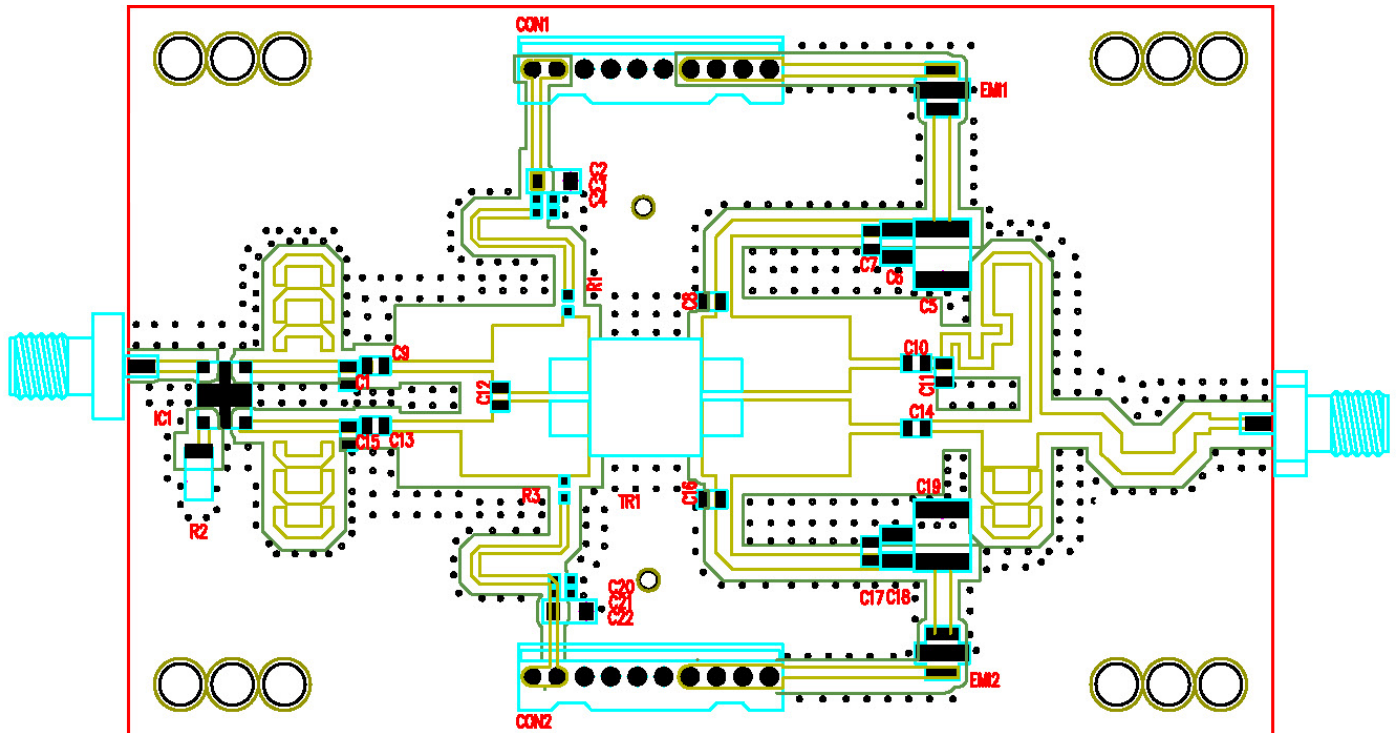
Typical Small Signal Performance

(Tc=25 °C, Measured in the IE19195WD Doherty test board amplifier circuit)



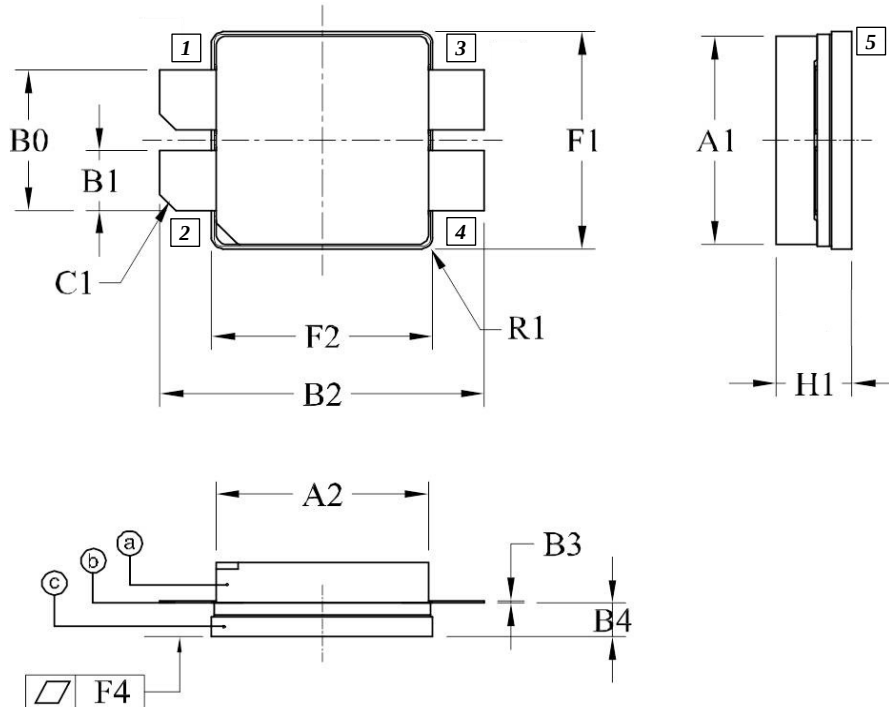
$P_{IN} = 0dBm$, $V_{DS} = 48V$, $I_{DQ} = 350mA$, $V_{GS(P)} = -5V$

Test Board Component Layout



Part	Description	Part Number	Manufacturer
R1,R3	20 ohm Chip Resistor	MCR10EZHZJ200	ROHM
R2	50 ohm Power Resistor	45-0040S	DICONEX
C2,C22	1nF Chip Capacitor	GRM216R71H102KA01D	MURATA
C3,C21	100pF Chip Capacitor	GRM1885C1H100JA01D	MURATA
C4,C20	10pF Chip Capacitor	GRM1885C1H100JA01D	MURATA
C1	1.8pF High Q Capacitor	201 CHA 1R8 CSLE	TEMEX
C9,C13	6.8pF High Q Capacitor	201 CHA 6R8 CSLE	TEMEX
C15	2pF High Q Capacitor	201 CHA 2R0 CSLE	TEMEX
C12	1.2pF High Q Capacitor	201 CHA 1R2 BSLE	TEMEX
C5,C19	10uF MLCC	CKG57NX7R2A106MT	TDK
C8	27pF High Q Capacitor	201 CHA 270 JSLE	TEMEX
C7,C16,C17	10pF High Q Capacitor	201 CHA 100 JSLE	TEMEX
C6,C18	2.2uF Chip Capacitor	GRM32ER72A225KA35L	MURATA
C10	3.9pF High Q Capacitor	201 CHA 3R9 CSLE	TEMEX
C11	0.1pF High Q Capacitor	201 CHA 0R1 BSLE	TEMEX
C14	3.3pF High Q Capacitor	201 CHA 3R3 CSLE	TEMEX
IC1	3dB HYBRID COUPLER, 1.7~2GHz, 80W	CMX19Q03	RN2
EMI1,EMI2	EMI FILTER	CTH32R102S20A-TM	MARUWA
CON1,CON2	DC Connector	5045-10	MOLEX
PCB	$\epsilon_r=3.48 \pm 0.05$, 0.030" (0.762mm)	RO4350B	ROGERS Corp.
TR1	195W GaN Dual Transistor	IE19195WD	RFHIC

Package Dimensions (Type:RF12001DKR3)



Pin Description	
Pin No	Function
1	Path A Gate
2	Path B Gate
3	Path A Drain
4	Path B Drain
5	Source

- (a)- Lid
 (b)- Lead Frame
 (c)- Flange

Dim.	INCH			MILLIMETER		
	MIN	TYP	MAX	MIN	TYP	MAX
A1	.379	.384	.389	9.63	9.76	9.89
A2	.379	.384	.389	9.63	9.76	9.89
B0	.253	.258	.263	6.43	6.56	6.69
B1	.104	.109	.115	2.65	2.78	2.91
B2	.567	.587	.606	14.40	14.90	15.40
B3	.003	.005	.007	0.08	0.13	0.18
B4	.057	.062	.067	1.44	1.57	1.70
C1 (Chamfer)	.024	.030	.035	0.62	0.75	0.88
F1	.395	.400	.405	10.03	10.16	10.29
F2	.395	.400	.405	10.03	10.16	10.29
F4	-	.001	-	-	0.03	-
H1	.115	.137	.158	2.92	3.47	4.02
R1 (Radius)	.016	.020	.024	0.40	0.50	0.60

Revision History

Part Number	Release Date	Version	Description	Data Sheet Status
IE19195WD	March, 2016	1.0	Modified Electrical Characteristics	-

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