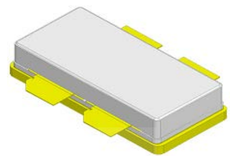
Product Features

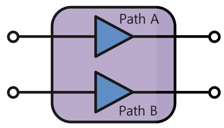
- 1805~1880MHz
- 250W Saturated Power @ 48V
- 57% Drain Efficiency @ 46.5dBm
- Internally Matched
- Asymmetrical Doherty GaN HEMT

Applications

- WiMAX, LTE, WCDMA, GSM
- Multi-Band, Multi-Mode
- Multi-Carrier
- High Efficiency, Doherty Amplifier



Package Type : RF24001DKR3



Typical Single-Carrier LTE Performance

(V_{DS}= +48V, T_C=25℃, 50Ω)

Frequency [MHz]	Peak Power	Average Power*1			
	Power [W]	Power [W]	Gain [dB]	Drain Efficiency [%]	ACLR [dBc]
1810.0	306.2	45	16.8	57.8	-23.9
1842.5	291.7	45	16.7	58.2	-26.7
1875.0	260.6	45	16.5	56.9	-28.7

Note

*1 Measured in the IE18250D Doherty test board amplifier circuit, under LTE 10MHz, PAR 7.5dB @0.01% probability on CCDF.

Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Condition
Drain to Source Voltage	V_{DSS}	150	V	Tc=25℃
Gate to Source Voltage	V_{GS}	-10, +2	V	Tc=25℃
Operating Voltage	V_{DD}	52	V_{DC}	-
Storage Temperature	T_{STG}	-65, +150	℃	-
Case Operating Temperature	T_C	-40, +150	℃	30 seconds
Operating Junction Temperature*1	T_J	225	℃	-
Soldering Temperature*2	T_S	245	℃	-

Note

*1 Continuous use at maximum temperature will affect MTTF.

*2 Refer to the Application Note(AN-002) on soldering - "Solder Condition for RFHIC's GaN Device"

Thermal Characteristics

Rating	Symbol	Value	Unit	Condition
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.90 *1	℃/W	Tc=85℃

Note

*1 Measured for the IE18250D at dissipation power of 48.3W.

Electrical Characteristics (T_C=25℃ unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
DC Characteristics - Path A (Carrier)*1						
Maximum Forward Gate Current	Tc= 25℃	I_{GMAX}	-	-	12	mA
Maximum Drain Current*2	Tc= 25℃	I_{DMAX}	-	-	4.5	A
Power Dissipation	Tc= 85℃	P_{DMAX}	-	-	48.3	W
Gate Threshold Voltage	V_{DS} = 10V I_D = 10.8mA	$V_{GS(TH)}$	-3.8	-3.0	-2.3	V_{DC}
Gate Quiescent Voltage	V_{DS} = 48V I_D = 350mA	$V_{GS(Q)}$	-	-2.7	-	V_{DC}
Drain-Source Breakdown Voltage	V_{GS} = -8V I_D = 10.8mA	V_{BR}	150	-	-	V
Saturated Drain Current*3	V_{DS} = 6V V_{GS} = 2V	I_{DS}	9.0	10.8	-	A
Gate Leakage Current	V_{GS} = -8V V_{DS} = 120V	I_{GLKG}	-2.4	-	-	mA
Drain Leakage Current	V_{GS} = -8V V_{DS} = 120V	I_{DLKG}	-	-	4.3	mA
DC Characteristics - Path B (Peaking)*1						
Maximum Forward Gate Current	Tc= 25℃	I_{GMAX}	-	-	24	mA
Maximum Drain Current*2	Tc= 25℃	I_{DMAX}	-	-	9.0	A
Power Dissipation	Tc= 85℃	P_{DMAX}	-	-	84.8	W
Gate Threshold Voltage	V_{DS} = 10V I_D = 21.6mA	$V_{GS(TH)}$	-3.8	-3.0	-2.3	V_{DC}
Gate Quiescent Voltage	V_{DS} = 48V I_D = 750mA	$V_{GS(Q)}$	-	-2.7	-	V_{DC}
Drain-Source Breakdown Voltage	V_{GS} = -8V I_D = 21.6mA	V_{BR}	150	-	-	V
Saturated Drain Current*3	V_{DS} = 6V V_{GS} = 2V	I_{DS}	18.0	21.6	-	A
Gate Leakage Current	V_{GS} = -8V V_{DS} = 120V	I_{GLKG}	-4.8	-	-	mA
Drain Leakage Current	V_{GS} = -8V V_{DS} = 120V	I_{DLKG}	-	-	8.6	mA

Note

*1 Measured on wafer prior to packaging.

*2 Current Limit for long term, reliable operation.

*3 Scaled from PCM data.

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
RF Characteristics (Fc=1842.5MHz unless otherwise noted)						
Saturated Output Power[*1,4]	V_{DS} = 48V I_{DQ} = 350mA	P_{SAT}	-	250	-	W
Modulated Gain[*2]	V_{DS} = 48V I_{DQ} = 350mA P_{OUT} = 46.5dBm	G_{BR}	15.0	16.5	-	dB
LTE Linearity[*2]	V_{DS} = 48V I_{DQ} = 350mA P_{OUT} = 46.5dBm	ACLR	-	-25.0	-23.0	dBc
Modulated Drain Efficiency[*2]	V_{DS} = 48V I_{DQ} = 350mA P_{OUT} = 46.5dBm	η	54.0	57.0	-	%
Output Mismatch Stress[*1, 3]	V_{DS} = 48V I_{DQ} = 350mA P_{OUT} = P_{SAT} Pulsed	VSWR	10:1	-	-	ψ

Note

*1 Pulse width 100μsec, Duty Cycle 10%.

*2 Measured in the IE18250D Doherty test board amplifier circuit, under LTE 10MHz, PAR7.5dB @0.01% probability on CCDF.

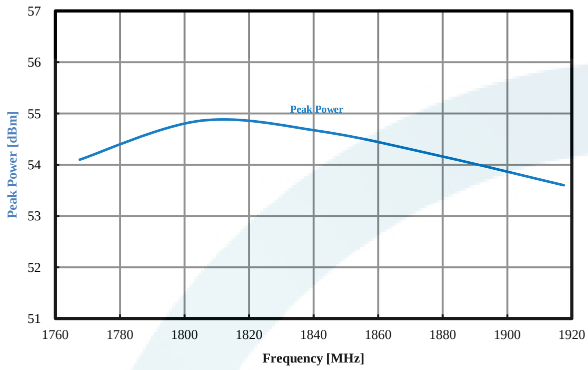
*3 Measured in the IE18250D Doherty test board amplifier circuit. No damage at all phase angles.

*4 Psat is defined as ∆Pout/∆Pin<0.1, where ∆Pin is increased input power, ∆Pout is increased output power.

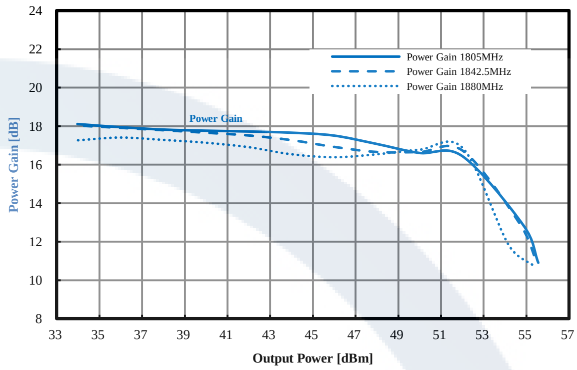
Typical Pulsed Signal Performance

(Tc=25℃, Measured in the IE18250D test board amplifier circuit)

Peak Power vs. Frequency



Pulsed Power Gain vs. Output Power

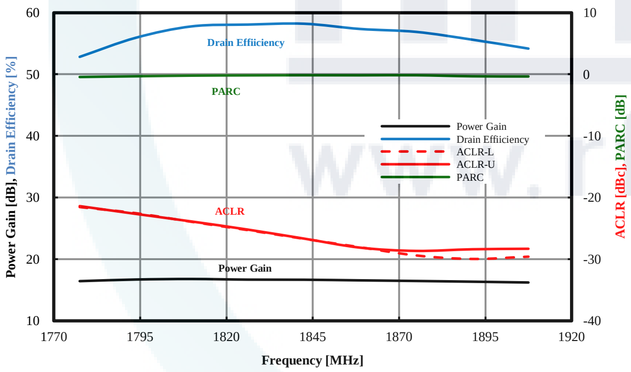


V_{DS} = 48V, $I_{DQ(C)}$ = 350mA, VGS(P)=-5V, Pulse Width = 100μsec, Duty Cycle = 10%

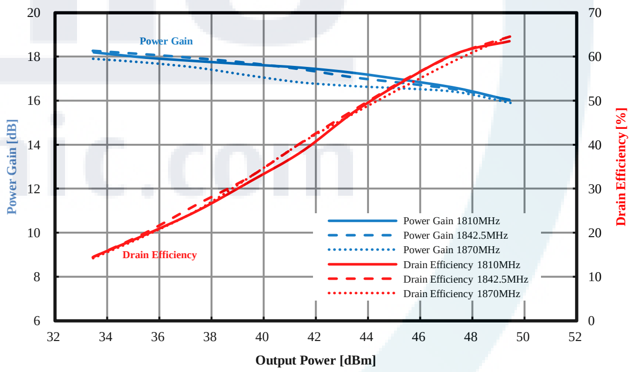
Typical LTE Signal Performance

(Tc=25℃, Measured in the IE18250D test board amplifier circuit)

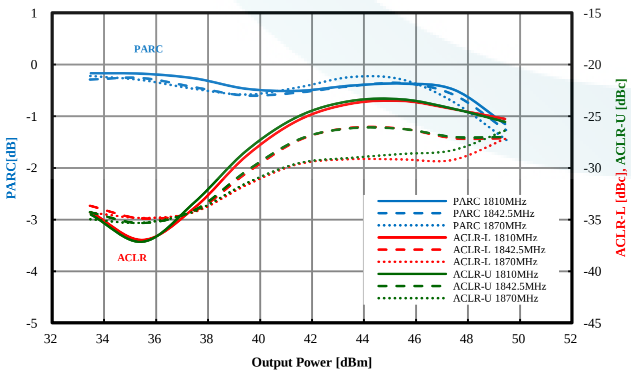
LTE Power Gain, Drain Efficiency, ACLR, PARC vs. Frequency



Power Gain, Drain Efficiency vs. Output Power



PARC, ACLR vs. Output Power

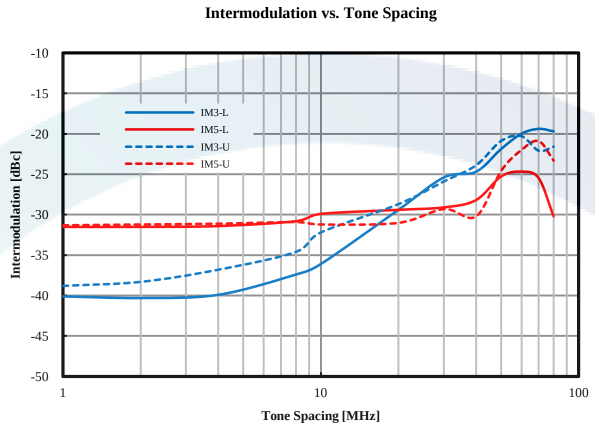


P_{AVG} = 46.5dBm, V_{DS} = 48V, $I_{DQ(C)}$ = 350mA, $V_{GS(P)}$ = -5V

LTE 10MHz BW, PAPR=7.5dB @ 0.01% Probability on CCDF

Typical 2-tone Intermodulation Imbalance Performance

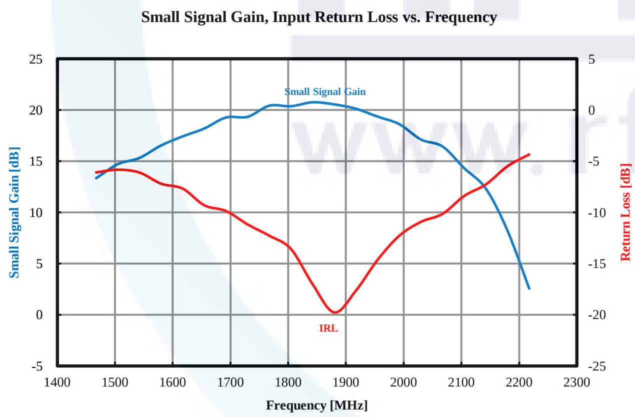
(Tc=25℃, Measured in the IE18250D Doherty test board amplifier circuit)

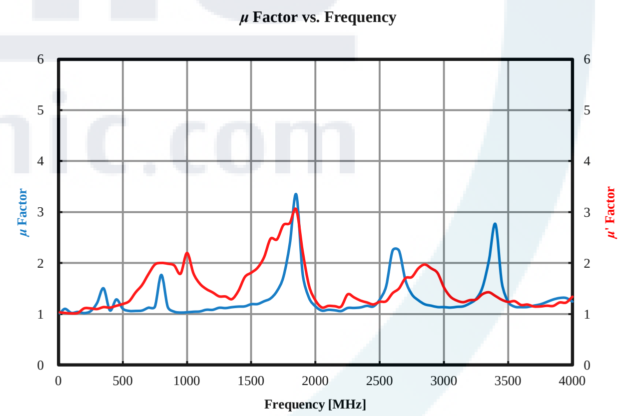


2-tone Power = 52.2dBm, V_{DS} = 48V, $I_{DQ(C)}$ = 350mA, $V_{GS(P)}$ = -5V

Typical Small Signal Performance

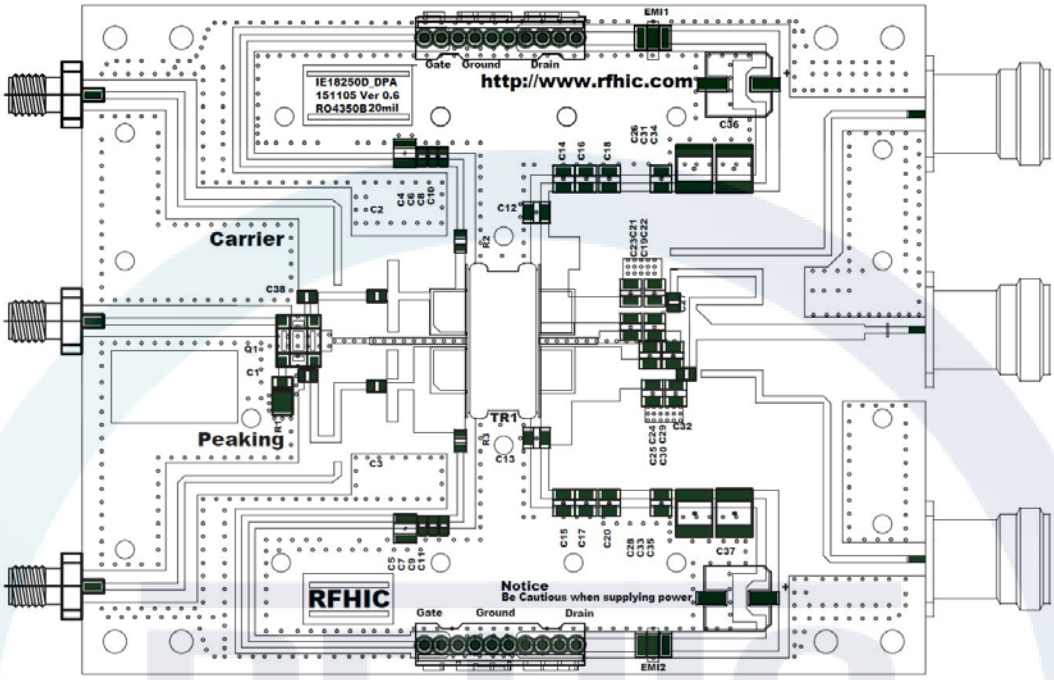
(Tc=25℃, Measured in the IE18250D Doherty test board amplifier circuit)





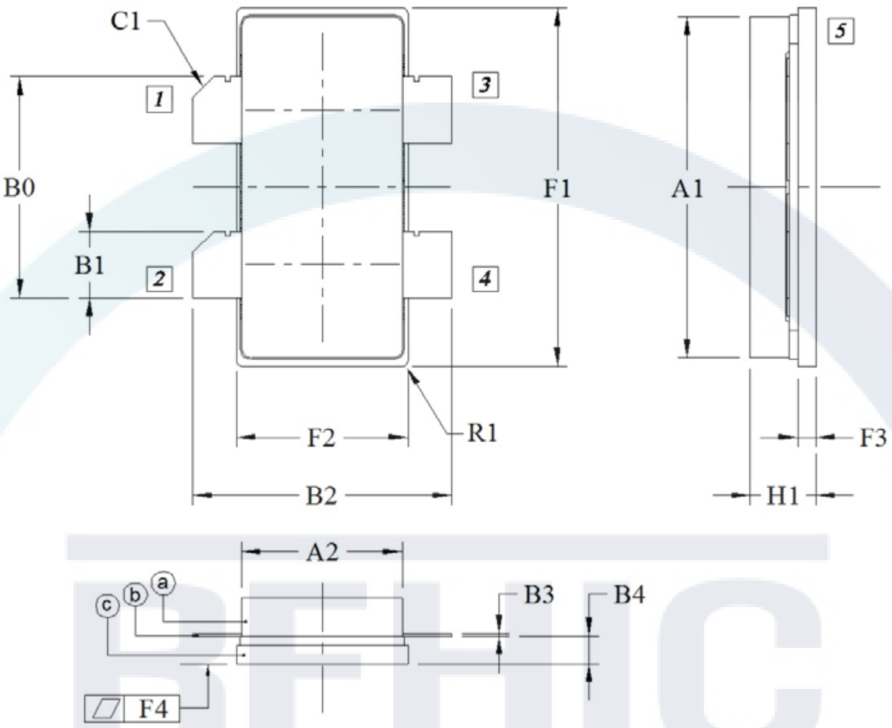
P_{IN} = 0dBm, V_{DS} = 48V, I_{DQ} = 350mA, $V_{GS(P)}$ = -5V

Test Board Component Layout



Part	Description	Part Number	Manufacturer
R1	50 ohm Power Resistor	S1020A	RN2
R2, R3	10 ohm Chip Resistor	MCR10EZHJ100	ROHM
C1	0.5pF High Q Capacitor	201CHA0R5BSLE	TEMEX
C2	8.2pF High Q Capacitor	201CHA8R2CSLE	TEMEX
C3	10pF High Q Capacitor	201CHA100CSLE	TEMEX
C4,C5	10uF Polymer Capacitor	TCJA106M016R0200	AVX
C6,C7	10nF Chip Capacitor	GRM188R71H103KA01D	MURATA
C8,C9	1nF Chip Capacitor	GRM188R71H102KA01D	MURATA
C10,C11	100pF Chip Capacitor	GRM1885C1H101JA01D	MURATA
C16	10pF High Q Capacitor	501CHB100JSLE	TEMEX
C15, C18, C20	100pF High Q Capacitor	201CHB101JSLE	TEMEX
C19	1.5pF High Q Capacitor	201CHB1R5CSLE	TEMEX
C22, C29	1.0pF High Q Capacitor	201CHB1R0BSLE	TEMEX
C30	1.2pF High Q Capacitor	201CHB1R2CSLE	TEMEX
C27	15pF High Q Capacitor	201CHA150JSLE	TEMEX
C32	33pF High Q Capacitor	201CHA330JSLE	TEMEX
C31, C33, C34, C35	10uF MLCC	RS80R2A106M	MURAWA
C36, C37	33uF Aluminum Capacitor	BDS100VC33MJ10TP	SAMYOUNG
C14, C21, C23, C24, C25 C26, C28	-	-	-
EMI1, EMI2	EMI FILTER	CTH32R102S20A-TM	MARUWA
Q1	Hybrid Coupler	CMX19Q03	RN2
CON1, CON2	DC Connector	22-04-1101	MOLEX
PCB	εr=3.66 ± 0.05, 0.020” (0.508mm)	RO4350B	ROGERS Corp.
TR1	250W GaN Transistor	IE18250D	RFHIC

Package Dimensions (Type:RF24001DKR3)



Pin Description	
Pin No	Function
1	Path A Gate
2	Path B Gate
3	Path A Drain
4	Path B Drain
5	Source

ⓐ- Lid

ⓑ- Lead Frame

ⓒ- Flange

Dim.	INCH			MILLIMETER		
	MIN	TYP	MAX	MIN	TYP	MAX
A1	0.767	0.772	0.777	19.48	19.61	19.74
A2	0.357	0.362	0.367	9.07	9.20	9.33
B0	0.495	0.500	0.505	12.57	12.70	12.83
B1	0.145	0.150	0.155	3.68	3.81	3.94
B2	0.580	0.584	0.589	14.72	14.84	14.97
B3	0.003	0.005	0.007	0.08	0.13	0.18
B4	0.057	0.062	0.067	1.44	1.57	1.70
C1 (Chamfer)	0.042	0.047	0.052	1.07	1.20	1.33
F1	0.806	0.811	0.816	20.47	20.60	20.73
F2	0.381	0.386	0.391	9.67	9.80	9.93
F3	0.031	0.036	0.041	0.79	0.92	1.05
F4	-	0.002	-	-	0.04	-
H1	0.127	0.148	0.170	3.22	3.77	4.32
R1 (Radius)	0.022	0.026	0.030	0.55	0.65	0.75

Revision History

Part Number	Release Date	Version	Description	Data Sheet Status
IE18250D	April, 2016	1.0	Initial Release of DataSheet	-